IN THE CLAIMS

Please amend claims 1, 4, 6-7, 11, 16, and 18 as follows:

1. (Currently Amended) In a data processing system having a processor responsively coupled to a store-in cache memory which is responsively coupled to a lower level memory, the improvement comprising:

a. A flush buffer ~~responsively~~ directly coupled to said store-in cache memory and said lower level memory.

2. (Original) A data processing system according to claim 1 further comprising a tag memory responsive coupled to said store-in cache memory which indicates whether a particular location within said store-in memory has been modified by said processor.

3. (Original) A data processing system according to claim 2 further comprising a logic circuit which loads said flush buffer with data from said particular location within said store-in cache memory in response to said indication that said particular location within said store-in memory has been modified by said processor.

4. (Currently Amended) A data processing system according to claim 3 wherein said flush buffer further comprises a first flush buffer store <u>having a first input and a first output</u> and a second flush buffer store <u>having a second input and a second output</u>.

5. (Original) A data processing system according to claim 4 further comprising a temporary register responsively coupled to said store-in cache memory, said first flush buffer store, and said second flush buffer store which routes said data from said particular location to an available one of said first flush buffer store and said second flush buffer store.

6. (Currently Amended) A data processing system comprising:

a. A processor;

b. A store-in cache memory responsively coupled to said processor;

c. A lower level memory responsively coupled to said store-in cache memory; and

d. A flush buffer ~~responsively~~ <u>directly</u> coupled to said store-in cache memory and said lower level memory.

7. (Currently Amended) A data processing system according to claim 6 wherein said flush buffer further comprises a first flush buffer store having a first input and a first output and a second flush buffer store having a second input and a second output.

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8. (Original) A data processing system according to claim 7 further comprising:

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a. A temporary register responsively coupled to said store-in cache memory, said first flush buffer store, and said second flush buffer store.

9. (Original) A data processing system according to claim 8 further comprising:

a. A tag memory responsively coupled to said store-in cache memory for indicating whether a particular location has been modified by said processor.

10. (Original) A data processing system according to claim 6 further comprising:

a. A logic circuit responsively coupled to said tag memory, said store-in cache memory, and said temporary register which routes data from said particular location from said store-in

cache memory to said temporary register when said indication is that said particular location has been modified by said processor.

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11. (Original) A method of flushing a store-in cache memory comprising:

a. Receiving a data request at said store-in cache memory;

b. Searching said store-in cache memory in response to said data request;

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c. Experiencing a cache miss in response to said searching step;

d. Selecting a particular location within said store-in cache memory to be flushed; and

e. Transferring data from said particular location to a flush buffer.

12. (Original) A method according to claim 11 further comprising:

a. Determining whether data within said particular location was modified by a processor.

13. (Original) A method according to claim 12 further comprising:

a. Inhibiting said transferring step if said determining step determines that said data within said particular location was not modified by said processor.

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14. (Original) A method according to claim 13 wherein said transferring step further comprises routing said data to the available one of a first flush buffer store and a second flush buffer store.

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15. (Original) A method according to claim 14 further comprising:

a. Rewriting said data to a lower level memory following said transferring step.

16. (Currently Amended) An apparatus comprising:

a. Means for executing program instructions;

b. Means responsively coupled to said executing means for caching data on a store-in basis; and

c. Means ~~responsively~~ directly coupled to said caching means for buffering data from said caching means to be flushed.

17. (Original) An apparatus according to claim 16 further comprising:

a. Means responsively coupled to said caching means for selecting said data to be flushed.

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18. (Currently Amended) An apparatus according to claim 17 wherein said buffering means further comprises a first means for storing <u>having a first input and a first output</u> and a second means for storing <u>having a second input and a second output</u>.

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19. (Original) An apparatus according to claim 18 further comprising:

a. Means responsively coupled to said first storing means and said second storing means for routing said data to the available one of said first storing means and said second storing means.

20. (Original) An apparatus according to claim 19 further comprising:

a. Means responsively coupled to said caching means for determining whether said data has been modified by said executing means; and

b. Means responsively coupled to said determining means and said buffering means for inhibiting transfer of data from said caching means to said buffering means if said determining means

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determines that said data has not been modified by said executing means.